REMARKS

Applicant has studied the Office Action dated October 3, 2002. It is submitted that the application is in condition for allowance. Claims 1-4, 6-16, 25-27, and 32-36 are pending. Reconsideration and allowance of the pending claims in view of the following remarks are respectfully requested.

As an initial matter, Applicant notes that the present Office Action includes the following statements: "The proposed drawing correction filed on 05 August 2002 is: approved by the Examiner. If approved, corrected drawings are required in reply to this Office Action." However, Applicant sent corrected formal drawings to the Examiner (in a Supplemental Response that was mailed on July 10, 2002), and did not file any proposed drawing correction on or around August 5, 2002. Accordingly, Applicant understands the Examiner's statements to mean that the corrected formal drawings were approved, and that no further action on the drawings is necessary.

Turning to the patentability of the application, claims 1-4, 6, 7, 10, 13, 25-27, 32, 33, 35, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. (U.S. Patent No. 5,652,156) in view of Gardiner et al. (U.S. Patent No. 4,354,309). Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. in view of Gardiner et al. and Shih et al. (U.S. Patent No. 5,943,569). Claims 9 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao in view of Gardiner et al., Shih et al., and Wang et al. (U.S. Patent No. 5,646,061). Claims 12, 15, 16, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liao et al. in view of Gardiner et al. and Hamasaki (U.S. Patent No. 6,274,401). These rejections are respectfully traversed.

The present invention is directed to in-situ deposition and doping methods for polycrystalline silicon layers that prevent the dopant from reaching the surface during a subsequent thermal treatment. One preferred embodiment of the present invention provides an

in-situ deposition and doping method for a polycrystalline silicon layer of a semiconductor device. According to the method, a first intermediate layer of in-situ doped polycrystalline silicon is grown in a deposition chamber with a first thickness and a first doping level. After the first intermediate layer is grown, the deposition chamber is purged by stopping all gas flow into the chamber and pumping residual gas out of the chamber, so as to remove all available dopant.

After purging the deposition chamber, a second additional layer of polycrystalline silicon is grown with a second thickness and a second doping level that is lower than the first doping level. The first thickness is greater than the second thickness. Because there is provided the thinner and less doped second layer of polycrystalline silicon, the dopant is prevented from reaching the surface during a subsequent thermal treatment. Accordingly, the present invention provides an improved method for forming an in-situ doped polycrystalline silicon layer for a semiconductor device.

The Liao reference discloses a process for forming a multilayered gate that inhibits ion penetration to the underlying gate oxide layer. The Gardiner reference discloses a process for forming a multilayer polycrystalline silicon gate that reduces void formation. However, neither Liao nor Gardiner discloses an in-situ deposition and doping method for a polycrystalline silicon layer in which a first intermediate layer of in-situ doped polycrystalline silicon is grown with a first thickness and a first doping level, and then a second additional layer of polycrystalline silicon is grown with a lower second thickness and a lower second doping level, as is recited in independent claim 1. Independent claims 15, 25, and 33 contain similar recitations.

The Liao reference discloses a process for forming a multilayered gate by alternately depositing amorphous silicon layers and polycrystalline silicon layers. In particular, a first layer of amorphous silicon is deposited on an oxide layer, a second layer of polycrystalline silicon is deposited on the amorphous silicon layer, and then a third layer of amorphous silicon is deposited on the polycrystalline silicon layer. The alternating layers of amorphous silicon and polycrystalline silicon are sequentially grown in such a way as to have some mismatches among the grain boundaries of the different layers in order to slow diffusion of implanted dopant during

subsequent processing. Thus, Liao discloses forming a multilayer gate by depositing polycrystalline silicon layers on amorphous silicon layers so as to producing alternating layers of amorphous silicon and polycrystalline silicon.

In contrast, in embodiments of the present invention, two polycrystalline silicon layers are grown. More specifically, a first intermediate layer of in-situ doped polycrystalline silicon is grown, the deposition chamber is purged, and then a second additional layer of polycrystalline silicon is grown. Thus, in embodiments of the present invention, both the first and second layers are formed of identical polycrystalline silicon, apart from small differences induced by the different doping levels.

Liao does not teach or suggest growing a first polycrystalline silicon layer, purging the deposition chamber, and then growing a second polycrystalline silicon layer. Liao only teaches depositing alternating layers of amorphous silicon and polycrystalline silicon. Liao does state that "[t]he first layer grown may be polysilicon rather than amorphous silicon." However, this statement only discloses that it is a possible to invert the order of the layers (i.e., to deposit a second amorphous silicon layer over a first polycrystalline silicon layer), not that both the first and second layers can be made of polycrystalline silicon. This is made abundantly clear in the true following line of Liao that states: "The key feature of the invention is that the different types of layers alternate." Liao at 3:14-15. Further, adjacent layers must include an amorphous layer and a polycrystalline silicon layer, because otherwise Liao's purpose of exploiting the mismatch of the grain boundaries between layers to inhibit ion penetration would not be achieved.

Accordingly, Liao does not teach or suggest the claimed feature of growing two polycrystalline silicon layers. Furthermore, as recognized by the Examiner, Liao does not teach or suggest growing in-situ doped polycrystalline silicon layers, that the doping level of the second layer is lower than the doping level of the first layer, or that the thickness of the first layer is greater than the thickness of the second layer.

The Gardiner reference discloses a process for forming a multilayer gate by depositing increasingly doped layers of polycrystalline silicon. In particular, a first intrinsic (non-doped) layer of polycrystalline silicon is deposited, a second moderately doped layer of polycrystalline

silicon is deposited, and then a third strongly doped layer of polycrystalline silicon is deposited. The dopant is then diffused through the three layers by subsequent thermal processes. The three layers all have the same thickness (1000 Å), so the resulting average doping level is approximately 1/3 of the doping of the strongly doped third layer. Thus, Gardiner discloses forming a multilayer gate by depositing three polycrystalline silicon layers having the same thicknesses but with doping levels that increase in the order of deposition.

In contrast, in embodiments of the present invention, a first intermediate layer of in-situ doped polycrystalline silicon is grown, the deposition chamber is purged, and then a second additional layer of polycrystalline silicon is grown. The thickness of the first layer is greater than the thickness of the second layer, and the doping level of the second layer is lower than the doping level of the first layer. Thus, in embodiments of the present invention, a first polycrystalline silicon layer is formed, and then a thinner and less doped second polycrystalline silicon layer is formed.

Gardiner does not teach or suggest growing a first polycrystalline silicon layer, purging the deposition chamber, and then growing a thinner and less doped second polycrystalline silicon layer. While Gardiner may generally disclose depositing in-situ doped polycrystalline silicon layers having different doping levels, Gardiner specifically teaches a process in which the second layer has a greater doping level than the first layer, and the third layer has a greater doping level than the second layer. In other words, Gardiner teaches that each layer of polycrystalline silicon is deposited with a higher doping level than the previously-deposited layers. Thus, Gardiner actually teaches away from the claimed feature of growing a second polycrystalline silicon layer that is less doped than the previously-grown layer. The Examiner cannot make out a case of obviousness by altering the teachings of Gardiner so as to include a feature that is specifically taught away from by the reference itself. Further, if the process of Gardiner is altered so that a less-doped polycrystalline silicon layer is deposited over a higher-doped polycrystalline silicon layer, then Gardiner's purpose of reducing void formation in the lower layer so as to inhibit degradation of the underlying gate oxide layer during subsequent processing would not be achieved. The Examiner cannot altering the process disclosed in Gardiner so as to render it unsatisfactory for its intended purpose or change it principle of operation.

Accordingly, neither Liao nor Gardiner teaches or suggests the claimed features of growing a first in-situ doped polycrystalline silicon layer, and then growing a second in-situ doped polycrystalline silicon layer with a lower doping level and a lesser thickness. Furthermore, the disclosure of Gardiner prohibits any modification (of Gardiner itself or the combination of Liao and Gardiner) that would encompass the claimed feature of growing a second in-situ doped polycrystalline silicon layer with a lower doping level than a previously-grown first in-situ doped polycrystalline silicon layer.

The Examiner also took the position that it would be a matter of routine optimization by one of ordinary skill in the art to choose particular thicknesses and doping levels because such depend on the desired device characteristics and dimensions. This position of the Examiner is respectfully traversed.

The claimed relative thicknesses and doping levels recited in the claims of the present invention are not merely optimized for a specific application from the general teachings of the cited references or any other reference. This is not a case of optimization of known teachings for a specific purpose, but is instead a novel solution to the well known problem described in the background section of the specification. This is made clear by the fact that the claimed features are a less in-situ doped and thinner second layer, while the cited references respectively teach non in-situ doped layers and increasingly doped layers, along with same thickness layers or increasing thickness layers. The claimed features simply cannot be mere routine optimizations of known characteristics and dimensions when the claimed features go in a different direction than the characteristics and dimensions that are taught.

Further, these claimed characteristics and dimensions are necessary to provide the advantages of the present invention. In particular, a thinner and less doped second polycrystalline silicon layer is required to prevent the dopant from reaching the surface during subsequent thermal treatment. The cited references do not overcome the problems described in the background section of the specification and fail to provide such an advantage. Thus, it is improper for the Examiner to say that the recited characteristics and dimensions are matters of routine optimization, and the Examiner must instead use what is actually disclosed in the prior

art itself to show that the claimed invention was taught or suggested by the prior art in order to properly reject claims. The Examiner cannot just state that any missing features are "maters of routine optimization". If such features are known and merely routine choices, then the Examiner should have no problem finding at least one prior art reference that teaches the general concept and does not teach away from the present invention.

Additionally, Applicant respectfully submits that one of ordinary skill in the art would not have had any motivation for combining the processes of the Liao and Gardiner references so as to produce the claimed in-situ deposition and doping methods for a polycrystalline silicon layer. It is well-settled that a reference must provide some motivation or reason for one of ordinary skill in the art (working without the benefit of hindsight reconstruction using the applicant's specification) to make the necessary changes in the disclosed device. The mere fact that a reference may be modified in the direction of the claimed invention does not make the modification obvious unless the reference expressly or impliedly teaches or suggests the desirability of the modification. In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984); Ex parte Clapp, 227 USPQ 972, 973 (Bd. App. 1985); Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. App. 1984).

The Examiner has taken the position that it would have been obvious to combine features of a process that uses doping by implantation from one reference with features of an in-situ doping process from another reference in order to produce one in-situ doping process. However, this is no more than a conclusory statement of obviousness. A semiconductor fabrication process that uses in-situ doping is simply much different than a semiconductor fabrication process that uses doping by implantation. These very different processes operate in completely different manners and require very different considerations and features. Further, neither Liao nor Gardiner suggests or provides any motivation for combining the processes disclosed in each to produce the claimed process. Some motivation for combining these different features of different types of processes in a specific manner must be shown in order to sustain a finding of obviousness.

Liao and Gardiner fail to meet the basic requirement for a finding of obviousness established by the courts in Gordon, Clapp, and Chicago Rawhide. There is simply no suggestion in Liao or Gardiner of combining selected features of one reference with the process of the other reference in order to produce the claimed invention. Applicant respectfully submits that there is no motivation for combining the Liao and Gardiner references as suggested by the Examiner, and that the Examiner is engaging in hindsight reconstruction of the claimed invention. Additionally, Applicant submits that the combination of the Liao and Gardiner references fails to render obvious the claimed invention.

Applicant believes that the differences between the Liao, Gardiner, and the present invention are clear in independent claims 1, 15, 25, and 33, which set forth in-situ deposition and doping methods according to various embodiments of the present invention. Therefore, claims 1, 15, 25, and 33 distinguish over the Liao and Gardiner references, and the rejections of these claims under 35 U.S.C.§ 103(a) should be withdrawn.

As discussed above, claims 1, 15, 25, and 33 distinguish over the Liao and Gardiner references. Furthermore, the claimed features of the present invention are not realized even if the teachings of Shih, Wang, and Hamasaki are incorporated into Liao and Gardiner.[1] None of Shih, Wang, and Hamasaki teaches or suggests the claimed features of the present invention that are absent from Liao and Gardiner. Thus, claims 1, 15, 25, and 33 distinguish over the Liao, Gardiner, Shih, Wang, and Hamasaki references, and thus, claims 2-4, 6-10, 12-14, and 27, claim 16, claims 26 and 32, and claims 34-36 (which depend from claims 1, 15, 25, and 33, respectively) also distinguish over the Liao, Gardiner, Shih, Wang, and Hamasaki references. Therefore, it is respectfully submitted that the rejections of claims 1-4, 6-10, 12-16, 25-27, and 32-36 under 35 U.S.C. § 103(a) should be withdrawn.

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[1] Applicant makes no statement as to whether such a combination is even proper.

Applicant notes that claim 11 was not rejected. Accordingly, it is submitted that claim 11 is in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

Date: April 3, 2003

By: [signature]

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